REMARKS

Rejections under 35 USC 112

The various rejecitons under 35 USC 112 in paragraphs 3, 4 and 5 of the Office Actiuon are respoctfully traversed.

Paragraph 1

Applicants agree that no parameter being tested is specified. Applicants regard such a limitation as being excessive and refuse to specify a particular parameter.

Paragraph 2.

Applicants have provided an antecedent.

Paragraph 3.

Applicants agree that no process step being tested is specified. Applicants regard such a limitation as being excessive, since the process step to be modified will depend on the parameter being tested, and refuse to specify a particular process step.

Applicants maintain that the claims fully meet the requirements of 35 USC 112 and request that the examiner supply an example in which the claims are defective.

103(a) Rejection

The rejection of claims 1 - 20 under 35 USC 103(a) is respectfully traversed on the grounds that they may not be patentably combined..

It is settled law that references may not be combined if the effect of the second reference would be to defeat the purpose of or to substantially interfere with the operation of the first reference.

In this case, the Voogel reference, a test circuit is provided on a wafer thereby providing "rapid identification of process problems" (Abstract, line 3); "What is needed is an improved test circuit and method for analyzisg test wafers that readily and reliably identifies and isolates fabrication defects, thereby facilitating rapid development and refinement of the fabrication process steps - - " (Col. 3, lines 16 - 20).

In short, a primary advantage of the Voogel reference is providing test results early in the process so that changes may be made without waiting for the time for the circuits to pass through the fab and be packaged.

In contrast, the Leedy reference requires that the cincuit be essentially complete before testing. It has to be complete through the back end in order to use the special test surface (col 3, lines 50 - 51, col 4, lines 8- 11, and especially col 6, lines 58 - 61).

In short, the Leedy reference has to have a complete circuit with all the back end, ready for packaging and testing (col 6, lines 60 - 61). The main purpose of the Leedy process is to replace defective transistors or logic blocks with spare ones and thereby increase yield. In addition, the lengthy process described by Leedy Col 6, line 62 - extending for a lengthy discussion) provides a specialized tester surface that is "key" to Leedy (col 6, line 60). Changing the fabrication process is of little or no importance to Leedy.

If the two references are combined as the Examiner suggests, the IC will have to be completed electrically, (so that the circuits work and the chip has the specialized tester surface) and ready for packaging (according to Leedy). This level of completeness is referred to in the claims as "electrical completion" and is excluded in claims 1 and 17. The tester surface is exclude in claim 20.

This requirement defeats the main purpose of Voogel that the test process provide rapid turnaround to improve the fabrication process.

In addition, Voogel requires separate test sites that are structurally different (have different circuits) from the ICs on the wafer, whereas Leedy operates with the normal logic blocks that are provided for the final IC (including the redundant modules).

If Leedy's method were followed, the test made by Voogel could not be performed because they require special test circuits than are not part of the logic blocks that Voogel uses.

In summary, the combination suggested by the examiner would defeat the purpose of Voogel because: a) the extra time to electrically complete the wafer would prevent the rapid turnaround that is important to Voogel; and b) the test performed by Voogel could not be done because the special test circuits would not be present.

The examiner's combination does not meet the claims

Even if the examiner's suggested combination were made, it would not meet claims 1, 17 and 20.

Claim 1 requires that:

1) the test is performed before electrical completion of the circuit. The combination according to Leedy requires that the test is done after electrical completion of the circuit. The phrase "before electrical completion" also excludes a wafer or chip with the specialized test surface that is essential to Leedy. If the examiner disagrees with the foregoing sentence, he is invited to suggest an examiner's amendment.

2) the test is done using transistors in a chip location, not in a test circuit in a separate location. (The examiner has made an error in his statement in paragraph 8 of the Office Action in the last paragraph of page 3. The passages cited do NOT have anything to do with the invention. Applicants note that the examiner has left out in his description that the test circuits are conventionally in the kerf, or in the case of Voogel, in a separate area of the wafer that is separated from the chip locations where the ICs are formed. The claims have a requirement that the tested wafers are in a chip location, i.e. not in a separate test location and therefore the passage cited does not have anything to do with the invention. Leedy does show modification of an IC, to substitute redundant elements, but without any test of the process parameters - only pass/fail on the output.

3) The combination suggested would have the specialized test surface of Leedy, which is excluded by the claims.

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,

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